UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/568,730	02/17/2006	Wolfgang Clemens	411000-147	7125

27162 7590 02/19/2009

CARELLA, BYRNE, BAIN, GILFILLAN, CECCHI,
STEWART & OLSTEIN
5 BECKER FARM ROAD
ROSELAND, NJ 07068

EXAMINER	
SINCLAIR, DAVID M	

ART UNIT	PAPER NUMBER
2831	

MAIL DATE	DELIVERY MODE
02/19/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/568,730	CLEMENS ET AL.	
	Examiner	Art Unit	
	DAVID M. SINCLAIR	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5 and 9-14* is/are rejected.

7)☒ Claim(s) *6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/24/2008 has been entered.

Specification

2. The disclosure is objected to because of the following informalities:

[0021a] – "Fig. 1e" should read "Fig. 1f"

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 11-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 claims "a second semiconductor layer located between said first and second electrodes and disposed on one of the sides of said insulator layer opposite said first semiconductor layer". It is unclear to the examiner how the second semiconductor layer is formed between the first electrode and insulating layer when the first electrode is in direct ohmic contact with the insulating layer.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 2-5, & 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. (5,038,184) in view of Aratani et al. (5,705,826).

In regards to claim 10,

Chiang '184 discloses an organic capacitor having voltage controlled capacitance (title), comprising a substrate (43 – fig. 14; C5:L10); a first electrode supported on the substrate forming a first capacitor plate (102a-102n – fig. 14; C8:L28), the first electrode defining a first electrode total area value the first electrode total area value being reduced by a plurality of spaced recesses in the first electrode and forming an electrode first surface area having a value corresponding to the reduced value (fig. 14); a semiconductor layer (47 – fig. 14; C5:L2-6 & 41) on the first electrode and in ohmic contact with the first electrode (fig. 14); an insulation layer (44 – fig. 14; C5:L28-29) on and in ohmic contact with the semiconductor layer (fig. 14); and a second electrode (101 – fig. 14; C8:L27) on and in ohmic contact with the insulation layer (fig. 14) and forming a second capacitor plate, the second electrode having a second surface area value larger than the first surface area (fig. 14). Chiang '184 fails to disclose the semiconductor layer is an organic material.

Aratani '826 discloses using an organic semiconductor in place of traditional semiconductor such as Si when forming electronic devices (background of the invention).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an organic semiconductor as taught by Aratani '826

as the semiconductor material of Chiang '184 to obtain a varactor that is less expensive to manufacture.

The limitations "wherein the concentration of free charge carriers in at least said first semiconductor layer is varied in a controlled manner by application of a voltage between said first and second electrodes, the concentration of said charge carriers determining the capacitance of the capacitor, and the concentration of said free charge carriers in at least said first semiconductor layer is additionally varied in a controlled manner by a frequency of the applied voltage" are inherently met as these limitations are properties of the above structure. When the structure recited in the references is substantially identical to that of the claims, claimed properties are presumed to be inherent.

In regards to claim 2,

The limitation "the variation of the concentration of said free charge carriers results in a variation of an effective spacing (a) of the electrodes serving as capacitor plates, and said effective spacing (a) functionally determines the capacitance" is a property of the above structure of claim 1 and is therefore inherently taught. When the structure recited in the references is substantially identical to that of the claims, claimed properties are presumed to be inherent.

In regards to claim 3,

The limitation "the variation of the concentration of said free charge carriers results in a variation of an effective plate surface area, and said effective plate surface area functionally determines the capacitance" is a property of the above structure of claim 1 and is therefore inherently taught. When the structure recited in the references is substantially identical to that of the claims, claimed properties are presumed to be inherent.

In regards to claim 4,

The references as applied above disclose all the limitations of claim 4 except at least one of said first and second electrodes is a structured electrode. However, Chiang '184 further discloses at least one of said first and second electrodes is a structured electrode (first electrode is structured – fig. 14).

In regards to claim 5,

The references as applied above disclose all the limitations of claim 5 except the at least one structured electrode is embedded in said semiconducting layer. However, Chiang '184 further discloses the at least one structured electrode is embedded in said semiconducting layer (fig. 14).

In regards to claim 9,

The references as applied above disclose all the limitations of claim 5 except at least one of said functional layers is a layer of an organic substance.

Aratani '826 discloses at least one of said functional layers is a layer of an organic substance (background of the invention).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an organic semiconductor as taught by Aratani '826 as the semiconductor material of Chiang '184 to obtain a varactor that is less expensive to manufacture.

In regards to claim 14,

Chiang '184 discloses an organic capacitor having voltage controlled capacitance (title), comprising a substrate (43 – fig. 14; C5:L10); a first electrode supported on the substrate forming a first capacitor plate (102a-102n – fig. 14; C8:L28), the first electrode defining a first electrode total area value the first electrode total area value being reduced by a plurality of spaced recesses in the first electrode and forming an electrode first surface area having a value corresponding to the reduced value (fig. 14); a semiconductor layer (47 – fig. 14; C5:L2-6 & 41) on the first electrode and in ohmic contact with the first electrode (fig. 14), which semiconductor layer is arranged to act as an insulator at relatively high frequencies in the MHz and GHz range; and a second electrode (101 – fig. 14; C8:L27) on forming a second capacitor plate, the second electrode having a second surface area value larger than the first surface area (fig. 14). Chiang

'184 fails to disclose the semiconductor layer is an organic material and in direct ohmic contact with the second electrode.

Aratani '826 discloses using an organic semiconductor in place of traditional semiconductor such as Si when forming electronic devices (background of the invention) and using aluminum as the gate electrodes so that an insulator layer is not required and both the first and second electrodes are in direct contact with the semiconductor layer (fig. 7; C8:L58-62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an organic semiconductor and aluminum gate electrodes as taught by Aratani '826 when manufacturing the capacitor of Chiang '184 to obtain a varactor that is less expensive to manufacture.

The limitations "wherein the concentration of free charge carriers in at least said semiconductor layer is varied in a controlled manner by application of a voltage between said first and second electrodes; wherein the concentration of said charge carriers determines the capacitance of the capacitor; and wherein the concentration of said free charge carriers in at least said semiconductor layer is additionally varied in a controlled manner by the frequency of the applied voltage" are inherently met as these limitations are properties of the above structure.

When the structure recited in the references is substantially identical to that of the claims, claimed properties are presumed to be inherent.

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aratani '826 in view of Kurosawa et al. (2004/0184216).

In regards to claim 14,

Aratani '826 discloses an organic FET, comprising: a substrate (1 – fig. 7; C11:L6); a first electrode (2 – fig. 7; C11:L8) supported on the substrate, the first electrode defining a first electrode total area value; an organic semiconductor layer (4 – fig. 7; C11:L11) on the first electrode and in ohmic contact with the first electrode, which semiconductor layer is arranged to act as an insulator at relatively high frequencies in the MHz and GHz range; and a second electrode (6 & 5 – fig. 7; C11:L14) on and in ohmic contact with the semiconductor layer on a side of the semiconductor layer opposite the first electrode and forming a second capacitor plate, the second electrode having a second surface area value larger than the first surface area (fig. 7). Aratani '826 fails to disclose a capacitor wherein the first electrode total area value being reduced by a plurality of spaced recesses in the first electrode and forming an electrode first surface area having a value corresponding to the reduced value.

Kurosawa '216 disclose connecting a plurality of MOS capacitors on a single substrate by electrically connecting the drains and sources of the MOSFETs

together and connecting the gates of the MOSFETs together giving a capacitor wherein a first electrode total area value being reduced by a plurality of spaced recesses in the first electrode and forming an electrode first surface area having a value corresponding to a reduced value (fig. 3; [0002]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a plurality of the FETs taught by Aratani '826 and electrically connect the sources and drains together and electrically connect the gates together as taught by Kurosawa '216 to obtain a FET based capacitor with a large capacitance density.

The limitations "wherein the concentration of free charge carriers in at least said semiconductor layer is varied in a controlled manner by application of a voltage between said first and second electrodes; wherein the concentration of said charge carriers determines the capacitance of the capacitor; and wherein the concentration of said free charge carriers in at least said semiconductor layer is additionally varied in a controlled manner by the frequency of the applied voltage" are inherently met as these limitations are properties of the above structure. When the structure recited in the references is substantially identical to that of the claims, claimed properties are presumed to be inherent.

Allowable Subject Matter

9. Claims 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID M. SINCLAIR whose telephone number is (571)270-5068. The examiner can normally be reached on Mon - Thurs. 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego F. Gutierrez can be reached on (571) 272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Diego Gutierrez/
Supervisory Patent Examiner, Art Unit 2831

/D. M. S./
Examiner, Art Unit 2831